Fine Pitch TSV Integration in Silicon Micropin-Fin Heat Sinks for 3D ICs

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Abstract

Future high performance 3D systems require a systematic co-design of their electrical interconnect network and their heat removal mechanism. This paper presents fine pitch (20µm) and high aspect ratio (18:1) TSVs integrated in a micropin-fin heat sink capable of removing power density of 100W/cm^2 and resulting in junction temperatures below 50 ºC.

Introduction

Recent advances in semiconductor technology have led to emergence of memory intensive computing applications, which require significantly larger hardware infrastructure at lower costs to become economically viable. The general trend shows high performance server installation costs to be significantly lower than their running costs, primarily in terms of their energy consumption [1]. Therefore it becomes important to mitigate this gap by developing technologies that are more energy efficient and deliver higher performance at lower energy costs. Three-dimensional IC technology is pursued by many with a promise to solve the above mentioned interconnect problems and to develop energy efficient computing platforms through 3D integration of logic, memory, and optoelectronic devices [2],[3],[4],[5].

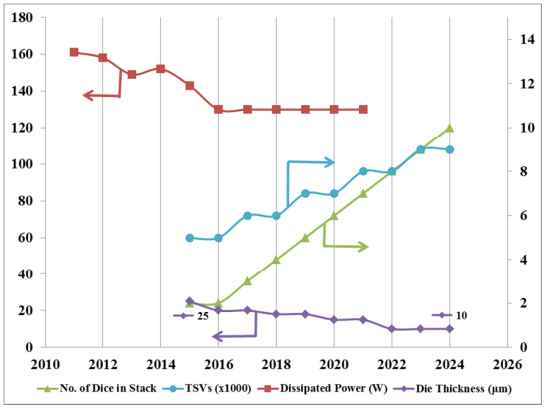

Figure 1: ITRS Roadmap for 2D/3D ICs [6].

ITRS projections for die thickness, TSV densities, dice per stack and dissipated power per die are plotted in Figure 1. While the power dissipation per die is projected to reduce, the number of dice in a 3D stack are expected to increase. The aggregate power density in 3D ICs is higher than what can be efficiently cooled through existing air-cooled heat sink technologies. Additionally, ITRS projects stacking 10 dice in a 3D stack by 2024 requiring higher density of power/ground TSVs in 3D ICs. High performance 3D ICs will benefit from microfluidic heat sink integrated with high bandwidth and low energy 3D interconnects between multiprocessors/cores and DRAMs to deliver economically viable high performance systems. The integration of fine pitch and high aspect ratio TSVs in staggered silicon micropin-fin heat sinks is discussed in this paper to address the electrical interconnect and heat removal problem simultaneously.

Heat Removal in 3D ICs

Thermal challenges in 3D ICs include high junction to ambient temperatures that lead to higher leakage power and localized hotspots that have much higher power densities. In 1981, a solution to the heat removal problem was proposed by Tuckerman and Pease [7]. The proposed microfluidic heat sink could provide cooling up to 790W/cm^2. One method to enhance single-phase cooling in such microfluidic heat sinks is to fabricate obstructions in the direction of liquid flow. A staggered circular micropin-fin structure (Figure 2) provides increased surface area, resulting in improved thermal resistance [8]. Previous work has shown the possibility of using liquid cooling instead of conventional air-cooling in 3D systems [9],[10] to provide efficient background heat removal. Such heat sinks can deal with increasing power dissipation in die stacks and assist other localized cooling technologies capable of dealing with hot spots [11],[12].

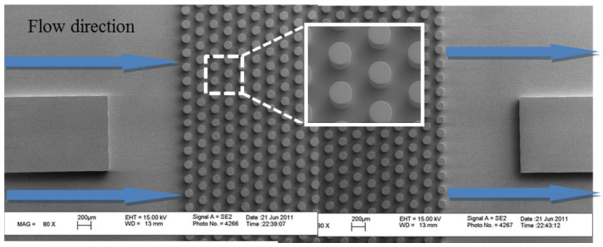

Figure 2: Staggered micropin-fin heat sink structure showing liquid flow direction.

Property	ACHS	MFHS (70 mL/min)
$R_{thermal}$ (measured) K cm^2/W	0.518	0.269
$R_{thermal}$ (model) K cm^2/W	-	0.274
Power Density (W/cm^2)	100.2	103.4

Table 1: Comparison of air cooled heat sink (ACHS) and microfluidic heat sink (MFHS).

The most important parameter that can be used to evaluate a MFHS design is its thermal resistance. In theory, the total thermal resistance (R_{tot}) consists of three parts: R_{cond} due to the conductance from the circuit through the substrate and heat sink interface; R_{conv} accounts for the convection from the heat sink to the liquid; R_{heat} is due to the increase of the fluidic temperature as it flows through the heat sink [13]. Table 1 shows the measured and simulated total thermal

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resistance for air cooled heat sink and micropin-fin heat sink at 100W/cm^2. The diameter, height and pitch of these micropin-fins are 150µm, 200µm and 225µm, respectively. Further benchmarking of air-cooled and micropin-fin heat sinks were done by measuring the junction temperatures at different power densities. This is compared to the ITRS projection for junction temperature requirements in Figure 3. Junction temperatures as low as 50ºC can be achieved at 100W/cm^2 using single phase staggered micropin-fin heat sinks.

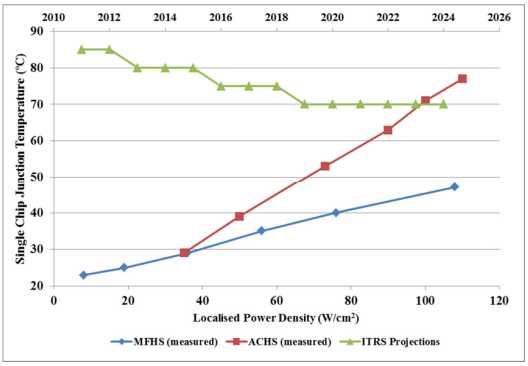

Figure 3: Benchmarking air cooled heat sinks (ACHS) and microfluidic heat sinks (MFHS) at flow rate of 70mL/min. Top axis represents ITRS projections for single chip junction temperature.

Electrical TSVs in Heat Sinks

Within the limited silicon area of the micropin-fins, an electrical interconnect solution is required that provides low-latency, high bandwidth and low energy-per-bit. This can be achieved by designing low capacitance TSVs. Additionally, such a solution should be able to cool the 3D system sufficiently.

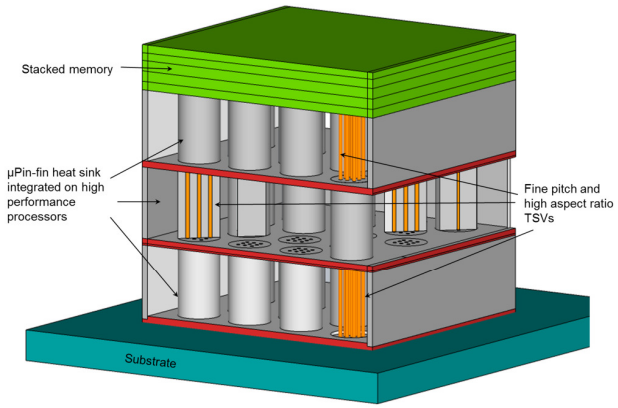

Figure 4: Schematic of micro-pinfin heat sink with integrated fine pitch and high aspect ratio TSVs.

Schematic of a high performance 3D system with micropin-fin heat sinks integrated with high performance multicore processor and multitier memory stack is shown in Figure 4. The integrated heat sink can efficiently remove the power dissipated in the high performance processors, while low power memory dice can be stacked without using integrated micropin-fin heat sink. The 3D system depicted here can deliver high performance while being able to communicate between the processor and the memory stacks using low parasitic and low energy interconnects.

An attempt to co-design the heat sink design while accounting TSV performance is shown in [9] and indicates that 3D connectivity of die stacks is challenged by two competing and enabling technologies (1) short electrical interconnects (TSVs) and (2) maximum surface area of microfluidic heat sink, and these need to be designed within the same silicon volume of the substrate. One advantage of using a staggered micropin-fin heat sink is the reduction in the micropin-fin height for the same thermal resistance of the heat sink. As shown in Figure 5, when TSV aspect ratio is limited (generally due to etching/processing), increasing the micropin-fin height also increases the TSV diameter, which translates to a quadratic increase in TSV area. By increasing the TSV aspect ratio, smaller diameter TSVs can be fabricated that have relatively smaller capacitance. Therefore, the height reduction from micropin-fin heat sinks combined with high aspect ratio TSVs can provide a lower-energy interconnect solution. Simulations were done to estimate TSV capacitance [14] and number density, by varying the TSV aspect ratio from 5 to 40 in a 200µm tall micropin-fin heat sink with 1% area dedicated for TSVs. High aspect ratio TSVs in micropin-fins can provide higher TSV densities and a corresponding reduction in their capacitance; further reduction in capacitance can be achieved through other means e.g. low-k dielectric liners. Therefore, the design of TSVs in micropin-fins requires careful analysis in order to extract the maximum electrical and thermal performance within the design limitations and integration challenges.

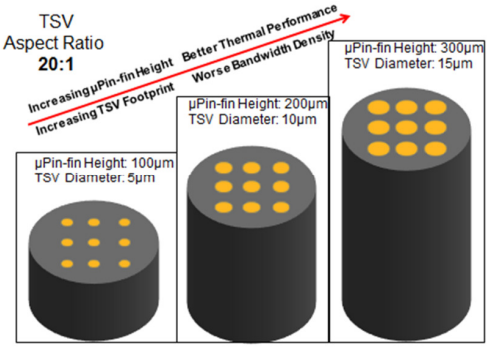

Figure 5: Impact of micropin-fin height on TSV density.

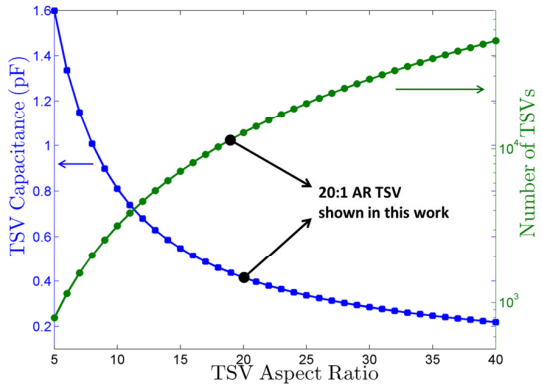

Figure 6: Impact of TSV aspect ratio on capacitance and TSV density in 200µm tall micropin-fins with 1µm SiO_2 sidewall liner. Number of TSVs is calculated in 1% of silicon area of 1cm^2 die.

Fabrication & Measurement

The fabrication of TSVs within micropin-fins starts with a 300µm thick double side polished silicon (DSP) wafer. High aspect ratio TSVs (~20:1) are fabricated using a standard Bosch process that alternates between SF_6 (plasma etch step) and inert C_4F_8 (deposition step). It may be noted here that to achieve the high aspect ratio the gas flow rate, cycle times and RF power is ramped over the process duration. Thermal oxide is then grown to isolate the TSVs from the substrate. Bottom-up pulsed electroplating with Enthone DVF plating solution is used to fill the vias with copper.

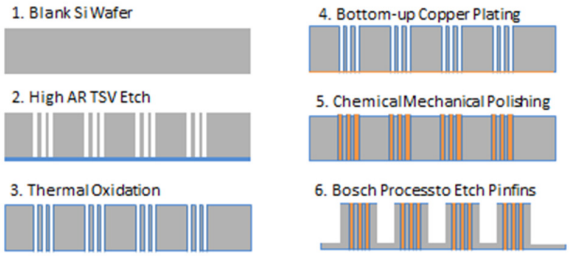

Figure 7: Fabrication process flow for TSVs in micropin-fins.

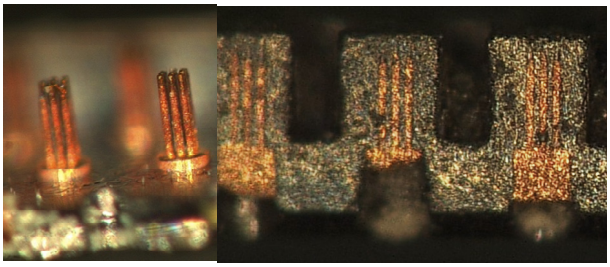

Figure 8: (Left) Free standing copper plated TSVs and (right) cross-sectional image of TSVs within the silicon micropin-fin heat sink.

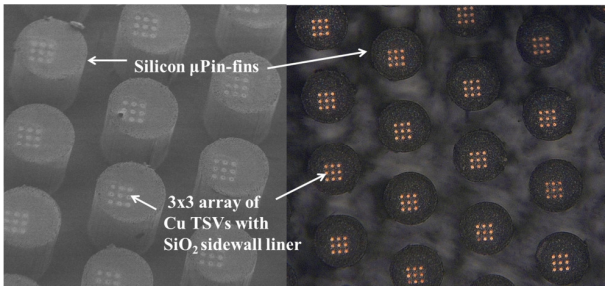

Figure 9: SEM (left) & optical images (right) of high aspect ratio TSVs integrated in micropin-fins (10µm diameter, 20µm pitch and 178 µm tall).

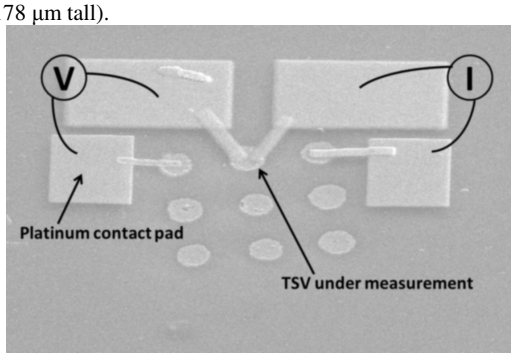

Figure 10: Resistance measurement of TSVs using four point technique. The platinum pads were deposited selectively using Focused Ion Beam (FIB) deposition.

Following electroplating, the sample is polished and excess silicon is removed using the Bosch process to make 200µm tall micropin-fins. The fabricated TSVs are ~10 µm in diameter and 178 µm deep (18:1). A summary of the fabrication process flow is shown in Figure 6. A cross-sectional view of the fabricated TSVs within the micropin-fin is shown in Figure 7. The TSVs are fully plated with no voids. The fabricated structure was dipped in KOH to remove any surrounding silicon; free standing high aspect ratio copper plated TSVs were observed. This shows the absence of voids in the electroplated TSVs. SEM and optical images of the fabricated structure are shown in Figure 9. The resistance of these TSVs was measured using four point technique; platinum pads were deposited selectively using Focused Ion Beam (FIB) deposition as shown in Figure 10. The theoretical value of TSV resistance for a 178µm tall TSV is 38 mΩ, this is within the error bar of the measured value of 36.5 ± 1.5 mΩ. In summary, a die spanning 10mm x 10mm can have 1,936 micropin-fins with diameter of 150µm at a pitch of 225µm. Each micropin-fin has 9 electrical TSVs, providing a total of 17,424 electrical I/Os can be used to connect adjacent layers of the 3D stack while using only 1.36% of the die area.

Conclusion

This work demonstrates a key enabling technology for energy efficient high performance 3D systems. Fine pitch TSVs were integrated within micropin-fins and their resistance was measured to be with reasonable error limits. These TSVs were integrated in a silicon micropin-fin heat sink that has been experimentally shown to remove 100W/cm^2 with junction temperatures below 50 ºC. Electrical performance metrics (e.g. bandwidth density and energy per bit) can be traded for thermal performance metrics (e.g. thermal resistance) by altering the micropin-fin design. This shows that the electrical and thermal design of next generation high performance 3D systems is inseparable and needs to be considered in a holistic manner to sustain performance gains in next-generation silicon technologies.

Acknowledgement

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